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EXAMINER	
AHMED, ENAM	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,175	RIDGEWAY ET AL.	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final

This is in response to applicants amendment filed on 4/16/08.

Response to applicants amendment

The applicants arguments have been fully considered, and are not found persuasive.

Response to applicants remarks

The applicant mentions on page 6, however Olnowich does not disclose a plurality of CRC calculation blocks performing separate n-bit CRC calculations in parallel where a switch selectively passes one of the n–bit CRC calculation values calculated by one of the CRC calculation blocks.

The Examiner disagrees with the statement, and points out the Olnowich reference teaches a parallel system in which CRC bytes are appended to messages on multiple nodes of a switch network, and then transmitted over a network which arrives at a receiving nodes where the CRC

bytes are regenerated. Thus, the Olnowich refrence teaches a plurality of CRC calculation blocks performing separate n-bit CRC calculations in parallel where a switch selectively passes one of the n–bit CRC calculation values calculated by one of the CRC calculation blocks (column 15, line 66 – column 16, line 20).

The applicant mentions on page 7, however, Olnowich does not disclose two separate CRC calculations in parallel and does not disclose calculating two separate CRC values in parallel that have a different number of bits.

The Examiner disagrees with the statement, and points out Olnowich teaches a plurality of nodes which are uni-direction or can be bi-directional, in which a message is appended with CRC bytes, and then transmitted over a network which arrives at a receiving nodes where the CRC bytes are regenerated. Thus, the Olnowich refrence teaches two separate CRC calculations in parallel and does not disclose calculating two separate CRC values in parallel that have a different number of bits (column 15, line 66 – column 16, line 20) and (column 8, line 55 – column 9, line 3).

35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 and 12-24 are rejected under 35 U.S.C. 102(b) as being unpatentable over Olnowich et al. (U.S. Patent No. 5,734,826).

With respect to claim 1, the Olnowich et al. reference teaches a plurality of CRC calculation blocks, each of the plurality of CRC calculation blocks performing a CRC calculation in parallel to yield a value of an n-bit CRC result (column 7, lines 18-23) and (column 8, lines 4-19); a switch for selectively passing one of the CRC calculation values calculated by one of said plurality of CRC calculation blocks (column 3, line 27 – column 4, line 7); a CRC register for latching the one of the CRC calculation values selectively passed by the switch (column 16, line 64 - column 17, line 31) and (column 18 , line 39 - column 19, line 9).

With respect to claim 2, the Olnowich et al. reference teaches wherein the latched CRC calculation value is inverted (column 18, line 67 – column 19, line 9).

With respect to claim 3, the Olnowich et al. reference teaches wherein the latched CRC calculation value is fedback to the plurality of CRC calculation blocks (column 17, lines 22-31) and (column 18, lines 58-67).

With respect to claim 4, the Olnowich et al. reference teaches wherein the plurality of CRC calculation blocks receives a data input (column 9, lines 56-62) and (column 15, lines 30-53).

With respect to claim 5, the Olnowich et al. reference teaches wherein the data input is in the form of one or more eight bit bytes (column 6, lines 49-58).

With respect to claim 6, the Olnowich et al. reference teaches wherein each of the plurality of CRC calculation blocks receives a different number of eight bit bytes from the data input (column 6, lines 49-58).

With respect to claim 7, the Olnowich et al. reference teaches wherein each of the plurality of CRC calculation blocks use a 32 bit CRC polynomial (column 7, lines 21-32).

With respect to claim 8, the Olnowich et al. reference teaches wherein each of the plurality of CRC calculation blocks uses the same 32 bit CRC polynomial (column 7, lines 21-32).

With respect to claim 12, the Olnowich et al. reference teaches wherein the 32 bit polynomial is loadable into the circuit (column 14, lines 29-30) and (column 14, lines 46-55).

With respect to claim 13, the Olnowich et al. reference teaches wherein the 32 bit polynomial is built into the circuit (column 4, lines 11-24).

With respect to claim 14, the Olnowich et al. reference teaches inputting a variable width data word (column 2, lines 14-21); calculating a first CRC value using the variable width data word and calculating a second CRC value using the variable width data word, wherein the first and second CRC value calculation occur in parallel (column 15, line 66 – column 16, line 54), (column 15, line 66 – column 16, line 20) and (column 8, line 55 – column 9, line 3).

With respect to claim 15, the Olnowich et al. reference teaches wherein the variable width data word is 32 bits long (column 7, lines 21-32).

With respect to claim 16, the Olnowich et al. reference teaches wherein the second CRC value is calculated using a portion of the variable width data word that is not used in the calculation of the first CRC value (column 16, lines 11-32).

With respect to claim 17, the Olnowich et al. reference teaches wherein the second CRC value is calculated using a portion of the variable width data word that is used in the calculation of the first CRC value (column 16, lines 11-32).

With respect to claim 18, the Olnowich et al. reference teaches selecting one of the first and second CRC values as the CRC output value (column 16, lines 21-50).

With respect to claim 19, the Olnowich et al. reference teaches feeding back the CRC output value as an input for the calculation of the first and second CRC values (column 16, lines 51-54).

With respect to claim 20, the Olnowich et al. reference teaches wherein the switch selection signal is a multi-bit value (column 16, lines 11-20).

With respect to claim 21, the Olnowich et al. reference teaches wherein the switch selection signal is a multi-bit value (column 17, lines 22-31).

With respect to claim 22, the Olnowich et al. reference teaches wherein the multi-bit value is decoded to provide a four bit value to a mux that performs the selection of the one of the first and second CRC values (column 17, lines 21-31).

With respect to claim 23, the Olnowich et al. reference teaches wherein the CRC output value is latched after being output by the mux and the latched CRC output value is fedback (column 16, line 64 – column 17, line 10).

With respect to claim 24, the Olnowich et al. reference teaches wherein the CRC output value is inverted (column 18, line 67 – column 19, line 9).

35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olnowich et al. (U.S. Patent No. 5,734,826) in view of Yang et al. (U.S. Patent No. 6,701,478).

With respect to claim 9, all of the limitations of claim 8 have been addressed. The Olnowich et al. reference does not teach wherein the 32 bit CRC polynomial is for ehternet. The Yang et al. reference teaches wherein the 32 bit CRC polynomial is for ehternet (column 3, lines 9 – 14). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Olnowich et al. and Yang et al. to incorporate wherein the 32 bit CRC polynomial is for ehternet into the claimed invention. The motivation for wherein the 32 bit CRC polynomial is for ehternet is for good error detection capabilities, and requires relatively little overhead (column 1, lines 42-43 – Yang et al. reference).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olnowich et al. (U.S. Patent No. 5,734,826) in view of Yamazaki et al. (U.S. Patent No. 6,487,686).

With respect to claim 10, all of the limitations of claim 5 have been addressed. The Olnowich et al. reference does not teach wherein there are sixteen CRC calculation blocks including the first and second CRC calculation blocks. The Yamazaki et al. reference teaches wherein there are sixteen CRC calculation blocks including the first and second CRC calculation blocks (column 5, lines 16-23) and (column 5, lines 35-42). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the references Olnowich et al. and Yamazaki et al. to incorporate wherein there are sixteen CRC calculation blocks including the first and second CRC calculation blocks into the claimed invention. The motivation for wherein there are sixteen CRC calculation blocks including the first and second CRC calculation blocks is so it would be possible to check an improvement of an error rate achieved by using the FEC error-correcting code (column 2, lines 12-14 – Yamazaki et al. reference).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olnowich et al. (U.S. Patent No. 5,734,826) in view of Abbott (U.S. Patent No. 6,351,142).

With respect to claim 11, all of the limitations of claim 1 have been addressed. The Olnowich et al. reference does not teach wherein the circuit is implemented as a field programable gate array. The Abbott reference teaches wherein the circuit is implemented as a field programmable gate array (column 2, lines 9-29). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the references Olnowich et

al. and Abbott to incorporate wherein the circuit is implemented as a field programmable gate array into the claimed invention. The motivation for wherein the circuit is implemented as a field programmable gate array so that the operations can be done at a lower, and more economical, clock rate (column 2, lines 27-29 - Abbott reference).

Conclusion

1. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

6/13/08

/JACQUES H LOUIS-JACQUES/

Supervisory Patent Examiner, Art Unit 2112